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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	2911.1US(96-0436.1)
First Inventor or Application Identifier	Jiang et al.
Title	GRAVITATIONALLY-ASSISTED CONTROL OF SPREAD OF VISCOUS MATERIAL APPLIED TO SEMICONDUCTOR ASSEMBLY COMPONENTS
Express Mail Label No.	EL248175219US

APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification Total Pages 24
(preferred arrangement set forth below)
-Descriptive title of the invention
-Cross References to related Applications
-Statement Regarding Fed Sponsored R&D
-Reference to Microfiche Appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings *(if filed)*
-Detailed Description
-Claim(s)
-Abstract of the Disclosure
3. ☒ Drawing(s) *(35 USC 113)* Total Sheets 17
4. Oath or Declaration Total Pages 2
a. ☐ Newly executed (original or copy)
b. ☒ Copy from a prior application (37 CFR 1.63(d))
(For continuation/divisional with Box 17 completed)
(Note Box 5 below)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☒ 37CFR 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure ☐ Copies of IDS
Statement (IDS/PTO-1449) Citations
12. ☒ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
14. ☐ Small Entity ☐ Statement filed in prior application,
Statement(s) Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(If foreign priority is claimed)
16. ☐ Other: . . . . . .
*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:
☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior Application No. 08/709,182
Prior application information: Examiner D. Graybill Group/Art Unit: 2814

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Tongbi Jiang; Syed S. Ahmad

Serial No.: To be assigned

Filed: April 21, 1999

For: GRAVITATIONALLY-ASSISTED CONTROL OF SPREAD OF VISCOUS MATERIAL APPLIED TO SEMICONDUCTOR ASSEMBLY COMPONENTS

Examiner: To be assigned

Group Art Unit: To be assigned

Attorney Docket No.: 2911.1US (96-436.1)

NOTICE OF EXPRESS MAILING
Express Mail Mailing Label Number: EL248175219US
Date of Deposit with USPS: April 21, 1999
Person making Deposit: Jared Turner

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the examination of the claims on the merits in the above-referenced application, please amend this application as follows:

IN THE SPECIFICATION:

Please amend the specification, as follows:

Page 3, line 10, change "on" to --in--.

Page 4, line 11, after ")" insert --,--.

Page 4, line 13, after "front" insert --,--.

Page 4, line 21, change "26" to --29--.

Page 5, line 4, change "for" to --from--.

Page 5, line 21, after "area" insert --or stencil cavity--.

Page 6, line 8, delete "the".

Page 6, line 8, delete "of".

Page 6, line 20, after "disposed" insert --in--.

Page 7, line 1, change "addition" to --additional--.

Page 7, line 8, change "requires" to --require--.

Page 8, line 1, change "via" to --vice--.

Page 8, line 6, change "require" to --requires--.

Page 8, line 14, after "," insert --such--.

Page 9, line 6, after "1002" insert --,--.

Page 10, line 7, after "is" insert --,--.

Page 10, line 7, after "course" insert --,--.

Page 10, line 15, change "dries or curing of" insert --dry or cure--.

Page 13, line 14, after "of" insert --the--.

Page 13, line 15, after "and" (2nd occur.) insert --the--.

Page 14, line 26, change "is" to --it--.

Page 15, line 17, delete "subsequent" (1st occur.).

Page 15, line 21, change "34" to --33--.

Page 15, line 24, change "34" to --33--.

Page 15, line 26, change "35" to --34--.

Page 16, line 11, after "reduced" insert --,--.

Page 16, line 21, after "polymer" insert --1007--.

IN THE CLAIMS:

Please cancel claims 1-6, 9-12, 17-20 and 22-24, without prejudice.

IN THE DRAWINGS:

A corrected informal FIG. 41 with changes in red ink is provided for the Examiner's approval. Element 1012 indicating the stencil opening was inadvertently omitted. This omission has been corrected in the enclosed formal drawings.

REMARKS

The Specification has been amended to correct inadvertent, typographical errors. No new subject matter has been added with the amendments to the specification.

FIG. 41 of the drawings has been amended to correct a minor, inadvertent error. No new matter has been added by this correction.

Respectfully submitted,

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Date: April 21, 1999

RGW/kf

PATENT
Attorney Docket 2911US(96-0436)

CERTIFICATION UNDER 37 C.F.R. § 1.10

EM096162529US — Express Mail Mailing Label No.
September 6, 1996 — Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Mathew Allen — Typed or printed name of person mailing application

Signature of person mailing application

APPLICATION FOR LETTERS PATENT

for

GRAVITATIONALLY-ASSISTED CONTROL OF SPREAD OF VISCOUS MATERIAL APPLIED TO SEMICONDUCTOR ASSEMBLY COMPONENTS

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GRAVITATIONALLY-ASSISTED CONTROL OF SPREAD OF VISCOUS MATERIAL APPLIED TO SEMICONDUCTOR ASSEMBLY COMPONENTS

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to maintaining the structure of viscous materials applied to semiconductor components. More particularly, the present invention relates to inverting electrical components formed from viscous materials or which include viscous materials in order to maintain the material boundary definition during baking, curing, and/or drying.

State of the Art: Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are goals of the computer industry. As components become smaller and smaller, tolerances for all semiconductor structures (circuitry traces, printed circuit board and flip chip bumps, adhesive structures for lead attachment, encapsulation structures, and the like) become more and more stringent. However, because of the characteristics of the materials (generally viscous materials) used in forming the semiconductor structures, it is becoming difficult to form smaller circuitry traces, conductive polymer bumps with closer pitches, adequate adhesive structures for leads attachment, and adequate encapsulation structures.

U.S. Patent 5,286,679 issued February 15, 1994 to Farnworth et al. ("the '679 patent"), assigned to the assignee of the present invention and hereby incorporated herein by reference, teaches attaching leads to a semiconductor device with adhesive in a "lead-over-chip" ("LOC") configuration. The '679 patent teaches applying a patterned thermoplastic or thermoset adhesive layer to a semiconductor wafer. The adhesive layer is patterned to keep the "streets" on the semiconductor wafer clear of adhesive for saw cutting and to keep the wire bonding pads on the individual dice clear of adhesive for wire bonding. Patterning of the adhesive layer is generally accomplished by hot or cold screen/stencil printing or dispensing by roll-on. Following the printing and baking of the adhesive layer on the semiconductor wafer, the individual dice are singulated from the semiconductor wafer. During packaging,

each adhesive coated die is attached to leadfingers of a lead frame by heating the adhesive layer and pressing the leadfingers onto the adhesive. If the adhesive layer is formed of a thermoset material, a separate oven cure is required. Furthermore, the adhesive layer may be formulated to function as an additional passivating/insulating layer or alpha barrier for protecting the packaged die.

Although the teaching of the '679 patent is a substantial advancement over previous methods for attaching leads in a LOC configuration, the miniaturization of the circuitry makes it difficult to achieve an adequate profile on the adhesive such that there is sufficient area on the top of the adhesive to attach the leadfingers. The process disclosed on the '679 patent is illustrated in FIGs. 23-29. FIG. 23 illustrates a side, cross-sectional view of a semiconductor substrate 602 with a bond pad 604, wherein a stencil or a screen print template 606 has been placed over the semiconductor substrate 602. The semiconductor substrate 602 is generally a wafer, although the term as used herein is not so restricted, and other substrate structures including silicon-on-insulator ("SOI") and printed circuit boards ("PCB") are specifically included. The stencil or screen print template 606 is patterned to clear the area around the bond pads 604 and to clear street areas 608 for saw cutting (i.e., for singulating the substrate into individual dice). An adhesive material 610 is applied to the stencil or screen print template 606, as shown in FIG. 24. Ideally, when the stencil or screen print template 606 is removed, adhesive prints 612 are formed with vertical sidewalls 614 and a planar upper surface 616, as shown in FIG. 25. However, since the adhesive material 610 must have sufficiently low viscosity to flow and fill the stencil or screen print template 606, as well as allow for the removal of the stencil or screen print template 606 without the adhesive material 610 sticking thereto, the adhesive material 610 of the adhesive prints 612 will spread, sag, or flow laterally under the force of gravity after the removal of the stencil or screen print template 606, as shown in FIG. 26. This post-application flow of adhesive material 610 can potentially cover all or a portion of the bond pads 604 or interfere with the singulating of the semiconductor wafer by flowing into the street areas 608.

Furthermore, and of even greater potential consequence than bond pad or street interference is the effect that the lateral flow or spread of adhesive material 610 has on the adhesive material upper surface 616. As shown in FIG. 27, the adhesive material upper surface 616 is the contact area for leadfingers 618 of a lead frame 620. The gravity-induced flow of the adhesive material 610 causes the once relatively well-defined edges 622 of the adhesive material to curve, resulting in a loss of surface area 624 (ideal shape shown in shadow) for the leadfingers 618 to attach. This loss of surface area 624 is particularly problematical for the adhesive print material upper surface 616 at the longitudinal ends 626 thereof. At the adhesive material longitudinal ends 626, the adhesive material flows in three directions (to both sides as well as longitudinally) causing a severe curvature 628, as shown in FIGs. 28 and 29. Stated are three ways the longitudinal ends of the adhesive print on patch flow in a 180° flow front resulting in blurring of the print boundaries into a curved perimeter. This curvature 628 results in complete or near complete loss of effective surface area on the adhesive material upper surface 616 for adhering the outermost leadfinger closest to the adhesive material end 626 (leadfinger 630). This results in what is known as a "dangling lead." Since the leadfinger 630 is not adequately attached to the adhesive material end 626, the leadfinger 630 will move or bounce when a wirebonding apparatus (not shown) attempts to attach a bond wire (not shown) between the leadfinger 630 and its respective bond pad 604 (shown from the side in FIG. 26). This movement can cause inadequate bonding or non-bonding between the bond wire and the leadfinger 630, resulting in the failure of the component due to a defective electrical connection.

LOC attachment can also be achieved by placing adhesive material on the leadfingers of the lead frame rather than on the semiconductor substrate. The adhesive material 702 is generally spray applied on an attachment surface 704 of leadfingers 706, as shown in FIG. 30. However, the viscous nature of the adhesive material 702 results in the adhesive material 702 flowing down the sides 708 of the leadfinger 706 and collecting on the reverse, bond wire surface 710 of the

leadfinger 706, as shown in FIG. 31. The adhesive material 702 which collects and cures on the bond wire surface 710 interferes with subsequent wirebonding which can result in a failure of the semiconductor component. The flow of adhesive material 702 for the attachment surface 704 to the bond wire surface 710 can be exacerbated if the leadfingers 706 are formed by a stamping process rather than by etching, the other widely employed alternative. The stamping process leaves a slight curvature 712 to edges 714 of at least one surface of the leadfinger 706, as shown in FIG. 32. If an edge curvature 712 is proximate the leadfinger attachment surface 704, the edge curvature 712 results in less resistance (i.e., less surface tension) to the flow of the adhesive material 702. This, of course, results in the potential for a greater amount of adhesive material 702 to flow to the bond wire surface 710.

Material flow problems also exist in application of encapsulation materials. After a semiconductor device is attached to a printed circuit board ("PCB") by any known chip-on-board ("COB") technique, the semiconductor device is usually encapsulated with a viscous liquid or gel insulative material (e.g., silicones, polyimides, epoxies, plastic, and the like). This encapsulation (depending on its formulation) allows the semiconductor device to better withstand exposure to a wide variety of environmental conditions such as moisture, ions, heat and abrasion.

One technique used in the industry is illustrated in FIGs. 33-35. A stencil 802 is placed on a conductor-carrying substrate or PCB 804 such that an open area 806 in the stencil 802 exposes a semiconductor device 808 to be encapsulated and a portion of the substrate or PCB 804 surrounding the semiconductor device 808, as shown in FIG. 33. An encapsulant material 810 is then extruded from a nozzle 812 into the stencil cavity 806, as shown in FIG. 34. However, when the stencil 802 is removed, the encapsulant material 810 sags or flows laterally under the force of gravity, as shown in FIG. 35. This flowing thins the encapsulant material 810 on the top surface 814 of the semiconductor device 808, which may result in inadequate protection for the semiconductor device 808. Using a thicker encapsulant material

would help minimize the amount of flow; however, thicker encapsulant materials are difficult to extrude through a nozzle and are subject to the formation of voids/air pockets. These voids/air pockets can cause delamination from the PCB 804 or the semiconductor device 808, and if the voids/air pockets contain water condensation, during subsequent processing steps the encapsulant material can be heated to the point at which the condensed water vaporizes, causing what is known as a "popcorn effect" (i.e., a small explosion) which damages (i.e., cracks) the encapsulation material, resulting in at least the contamination of and usually irreparable damage, effectively destroying the semiconductor device. Furthermore, using encapsulant materials with high thixotropic indexes may result in a concave shape which thins the encapsulant material 810 on the top surface 814 of the semiconductor device 808, which may result in inadequate protection for the semiconductor device 808, as shown in FIG. 36.

In an effort to cope with the encapsulant flow problem, the damming technique shown in FIGs. 37-40 has been used. A high viscosity material 902 is extruded through a nozzle 904 directly onto a substrate or PCB 906 to form a dam 908 around a semiconductor device 910, as shown in FIG. 37, or a stencil 912 can be placed on the substrate and PCB 906 such that a continuous aperture 914 in the stencil 912 exposes an area around the semiconductor device 910 to be dammed, as shown in FIG. 38. The high viscosity material 902 is then disposed the stencil aperture 914 to form the dam 908. A low viscosity encapsulation material 916 is then extruded into the area bounded by the dam 908 by a second nozzle 918, as shown in FIG. 39. The dam 908 prevents the low viscosity encapsulation material 916 from flowing, to form the dammed encapsulated structure 920 shown in FIG. 40 after curing. The dam 908 can be made with high viscosity material without adverse consequences since it does not directly contact the semiconductor device 910 or form any part, other than a damming function, of the encapsulation of the semiconductor device 910. Although this damming technique is an effective means of containing the low viscosity

encapsulation material 916, it requires addition processing steps and additional equipment, which increase the cost of the component.

Material flow problems further exist in forming conductive line and trace materials. As discussed in Liang et al., "Effect of Surface Energies on Screen Printing Resolution," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 2, May 1996 ("the Liang article"), miniaturization of semiconductor packages results in increased circuit densities which requires a proportionate reduction of the width of printed lines and traces on semiconductor substrates. However, there are two conflicting requirements for the conductive material applied in screen printing the printed lines and traces. The first requirement is that the conductive material should have sufficiently low viscosity to remove mesh marks and surface imperfections induced during the printing process. The conflicting requirement is that the conductive material should be sufficiently high in viscosity such that it does not flow excessively (i.e., spread). If the conductive material spreads, parallel lines could contact one another, resulting in a short. The Liang article investigates the influences of surface energies of the substrates and the conductive material on screen printing resolution. The conclusion of the Liang article is to use substrates with low surface energies, such as polymer-based substrates, to decrease the wettability of the conductive material to improve screen printing resolution. However, this approach limits the flexibility of using different substrate material for applications demanding different performance parameters. Furthermore, using polymer-based substrates may not be acceptable in certain applications such as high surface energy ceramic substrate.

Material flow problems further exist in forming conductive bumps on printed circuit boards and flip chips. Solder bumps, also termed "C4" bumps, for Controlled Collapse Chip Connection, are a conventional means for attaching and forming an electrical communication between a flip chip and a substrate or PCB, wherein the solder bumps are formed on the flip chip as a mirror-image of the connecting bond

pads on the PCB, or vis versa. The flip chip is bonded to the PCB by reflowing the solder bumps.

State-of-the-art solder bumps are generally made of multiple layers of various metals or metal alloys (e.g., lead, tin, copper) which will achieve an effective, strong and controlled-boundary bond between the substrate/PCB and the flip chip. However, the formation of these layered solder bumps require a substantial number of processing steps which increase the cost of the component. Furthermore, the solder bumps require a high temperature to reflow during the attachment of the flip chip to the substrate/PCB, which may damage temperature-sensitive components on the semiconductor device. Thus, solder bumps are being replaced by conductive polymer bumps.

As shown in FIG. 43, conductive polymer bumps 1002 are formed on bond pads 1004 on a semiconductor device substrate 1006. Alternatively, the bumps may be applied to a carrier substrate, as a PCB. The bond pads 1004 are in electrical communication with circuitry (not shown) on or in the semiconductor substrate 1006 via electrical traces 1008 (shown in shadow) in or on the semiconductor substrate 1006. The conductive polymer bumps 1002 are generally formed either by screen printing or stenciling. As shown in FIG. 41, a print screen or stencil 1010 is placed over the semiconductor substrate 1006 with openings 1012 over and aligned with each bond pad 1004. A conductive polymer 1007 is deposited in the openings 1012, as shown in FIG. 42. The print screen or stencil 1010 is then removed to form the conductive polymer bumps 1002, as shown in FIG. 43. The conductive polymer bumps 1002 are generally made from material which is sufficiently viscous that minimal material flow occurs when the print screen or stencil 1010 is removed. However, this self-minimization of flow is only applicable to specific limited ratios of height to width of the conductive polymer bumps 1002. If the height of the conductive polymer bump 1002 is too great relative to the width, the weight of the conductive material will cause the conductive polymer bump 1002 to collapse on itself and flow laterally. Thus, height-to-width ratios approaching the

preferred target of 3:1 or greater obtainable with solder bumps are unattainable with present methods. In short, to attain a satisfactory height of the conductive polymer bump 1002, the width of the conductive polymer bump 1002 must be increased proportionately. However, when the conductive polymer bump 1002 width is increased, for a given minimum pitch in spacing between adjacent conductive polymer bumps 1002 bond pad pitch also increases, which takes up more space on the semiconductor substrate 1006, limiting the number and arrangement of the die-to-carrier substrate connections. This is, of course, in conflict with the goal of miniaturizing semiconductor devices of ever-increasing circuit density.

Thus, it can be appreciated that it would be advantageous to develop a technique to control viscous material flow in the formation of semiconductor components while using commercially-available, widely-practiced semiconductor device fabrication techniques.

SUMMARY OF THE INVENTION

The present invention relates to a method for maintaining viscous material boundary definition by inverting electrical components formed from viscous materials or which include viscous materials during drying or curing.

The present invention comprises using standard techniques for applying viscous materials (e.g., spin on, spray on, roll on, screen printed, and the like) which form semiconductor device elements, such as circuitry traces, printed circuit board and flip chip bumps, adhesive structures for lead attachment, encapsulation structures, and the like. After application of the viscous materials on a semiconductor or carrier structure, the entire structure is flipped to an inverted position, followed by ambient or elevated temperature drying or curing. Rather than gravitational forces causing the viscous material to flow and expand as when upright and supported from below, the gravitational forces on the inverted semiconductor or carrier structure maintain the shape and boundary definition of the original viscous material formation. It has been found that inverting the semiconductor results in a substantial improvement for wall

SA 8/4/96 T.B 8/14/9

, reduction in corner radius of curvature

angles and improvement in the shape and boundary definition of the elements made from the viscous materials.

As a general matter, the entire structure is inverted immediately or as quickly as practical after the application of the viscous material to prevent any substantial spreading of the viscous material. This immediate inversion maximizes the benefit of the present invention by preserving the shape and boundary definition of the viscous material as applied. It is of course understood that the viscous material must be capable of adhering to the semiconductor or carrier structure and must not be of such a low viscous that it drips when inverted.

Furthermore, with regard to drying or curing, the structure need only be inverted until the viscous material has stabilized sufficiently to maintain its shape and boundary definition. Depending on the particular viscous material used, the minimum inversion time could be the time required to cure the outer surfaces of the viscous material such that a film is formed which contains the viscous material therein, or the minimum inversion time could be the time required to completely dries or curing of the viscous material element.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGs. 1-5 are a top plan and side cross sectional views of adhesive prints formed by the method of the present invention;

FIGs. 6-8 are schematic and graphical representations of experimental results comparing the lateral edges of an adhesive print formed by a prior art method and the method of the present invention;

FIGs. 9-11 are schematic and graphical representations of experimental results comparing the trailing edge of an adhesive print formed by a prior art method and the method of the present invention;

FIGs. 12-14 are schematic and graphical representations of experimental results comparing the leading edge of an adhesive print formed by a prior art method and the method of the present invention;

FIGs. 15-17 are cross-sectional views of a prior art wirebonded LOC semiconductor assembly;

FIG. 18 is a cross-sectional view of an encapsulated semiconductor device formed by the inversion method of the present invention;

FIGs. 19-21 are oblique views of the formation of traces on a semiconductor substrate by the method of the present invention;

FIG. 22 is a side cross-sectional view of a conductive polymer bump formed by the method of the present invention;

FIGs. 23-29 are side cross-sectional views of a technique of forming adhesive areas on a substrate for LOC attachment;

FIGs. 30-32 are side cross-sectional views of a technique of forming adhesive areas on leadfingers for LOC attachment;

FIGs. 33-35 are side cross-sectional views of a technique of forming an encapsulant layer on a semiconductor device;

FIG. 36 is a side cross-sectional view of an encapsulated semiconductor device with a concave shaped cured encapsulant;

FIGs. 37-40 are oblique views of techniques of forming an encapsulant layer on a semiconductor device using high viscosity material dams; and

FIGs. 41-43 are side cross-sectional views of a technique of forming conductive polymer bumps on a substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGs. 1-5 illustrate forming a rectangular adhesive print 102 on a semiconductor substrate 104. FIG. 1 shows several rectangular adhesive prints 102 uniformly distributed on the semiconductor substrate 104, such as a silicon wafer or SOI substrate. The spaces between the rectangular adhesive prints 102 can have a plurality of bond pads 108 disposed between a pair of rectangular adhesive prints 102. The spaces may also be void of any circuitry or structures to form vertical streets 110 and horizontal streets 112 along which a cutting saw proceeds to sever or singulate the semiconductor substrate 104 into individual semiconductor dice.

The rectangular adhesive prints 102 are generally formed in the manner discussed above for the '679 patent illustrated in FIG. 23-28. Referring to FIG. 24, when the adhesive material 610, such as thermoplastic adhesive materials including polyimides and thermosetting adhesive materials including phenolic resins, is applied to the stencil or screen print template 606, an adhesive material dispensing means, such as a spray nozzle, moves across the stencil or screen print template 606. Thus, as shown in FIG. 2, the adhesive material dispensing means moves in direction 114 forming the adhesive print 102 with two lateral edges 116 parallel with direction 114, and a trailing edge 118 and a leading edge 120 which are perpendicular with respect to direction 114.

As shown in FIG. 3, when the stencil or screen print template (shown in FIG. 24) is removed, the adhesive prints 102 are ideally formed with vertical sidewalls 122 and a planar upper surface 124. However, as previously discussed, the material forming the adhesive prints 102 must have sufficiently low viscosity to flow and fill the stencil or screen print template as well as to allow for the removal of the stencil or screen print template without the material forming the adhesive print 102 sticking to the stencil or screen print template and thus being lifted off the semiconductor substrate 104. Thus, the adhesive print 102 will flow laterally under the force of gravity after the removal of the stencil or screen print template, as shown in FIG. 4. This flow of the adhesive print 102 can potentially cover a portion of the

bond pads 108 or interfere with the singulating of the semiconductor wafer by flowing into the street areas 110, 112. This results in shortening street width W and decreasing gravity-reduced wall angle (α_G), which eventually creates problems with dicing the wafer, inference with bond pads, and dangled leadfingers (due to loss of surface area on a leadfinger attachment surface 128 on the adhesive print 102), as previously discussed.

The present invention inverts the semiconductor substrate 104 shortly after removal of the stencil or screen print template, as shown in FIG. 5. The inversion of the semiconductor substrate 104 results in gravitational force assisting in containing the flow and expansion of the adhesive prints 102 during drying or curing. The inversion of the semiconductor substrate 104 results in higher, inversion-contained wall angles (α_I) (also known as the "angle of repose"), wider street width W, and a greater surface area on the leadfinger attachment surface 128.

Experimental results have demonstrated that angles of leading edge, trailing edge and lateral edges of printed adhesives were increased and top surface area was also increased. FIGS. 6-8 illustrate the profile of the lateral edges 116. FIG. 6 illustrates the scan direction across two adjacent adhesive prints, a first adhesive print 130 and a second adhesive print 132. The scan 134 for the profiles shown in FIGs. 7 and 8 starts near lateral edge 136 of the first adhesive print 130, extends across the gap 138 between the first adhesive print 130 and the second adhesive print 132, and ends after a lateral edge 140 of the second adhesive print 132. It is noted that the z-axis (height) scales of FIGs. 7 and 8 have been expanded in a twenty (20) to one (1) ratio from the x-axis (scan length) scales to better show the details of the profiles. FIG. 7 shows a profile of the scan 134 of the first adhesive print 130 and the second adhesive print 132 formed by a conventional non-inversion method. FIG. 8 shows a profile of the scan 134 of the first adhesive print 130 and the second adhesive print 132 which were formed by the inversion method of the present invention. FIGs. 7 and 8 show that the lateral edge angles of repose have increased from α_G of 18.4 degrees (lateral edge 136) and 18.0 degrees (lateral edge 140) for the

non-inversion method to α_I of 22 degrees (lateral edge 136) and 20.6 degrees (lateral edge 140) for the inversion method of the present invention.

FIGs. 9-11 illustrate the profile of the trailing edge 118. FIG. 9 illustrates the scan direction across the adhesive print 102. The scan 142 for the profiles shown in FIGs. 10 and 11 starts prior to the trailing edge 118 of the adhesive print 102 and ends on the leadfinger attachment surface 128 of the adhesive print 102. It is noted that the z-axis (height) scales of FIGs. 10 and 11 have been expanded in a ten (10) to one (1) ratio from the x-axis (scan length) scales to better show the details of the profiles. FIG. 10 shows a profile of the scan 142 of the trailing edge 118 formed by a conventional non-inversion method. FIG. 11 shows a profile of the scan 142 of the trailing edge 118 formed by the inversion method of the present invention. FIGs. 10 and 11 show that the trailing edge angle of repose has increased from α_G of 9.0 degrees for the non-inversion method to α_G of 13.5 degrees for the inversion method of the present invention.

FIGs. 12-14 illustrate the profile of the leading edge 120. FIG. 12 illustrates the scan direction across the adhesive print 102. The scan 144 for the profiles shown in FIGs. 13 and 14 starts on the leadfinger attachment surface 128 of the adhesive print 102 and ends past the leading edge 120 of the adhesive print 102. It is noted that the z-axis (height) scales of FIGs. 13 and 14 have been expanded in a ten (10) to one (1) ratio from the x-axis (scan length) scales to better show the details of the profiles. FIG. 13 shows a profile of the scan 144 of the leading edge 120 formed by a conventional non-inversion method. FIG. 14 shows a profile of the scan 144 of the leading edge 120 formed by the inversion method of the present invention. FIGs. 13 and 14 show that the leading edge angle of repose has increased from 15.9 degrees for the non-inversion method to 22.6 degrees for the inversion method of the present invention.

From these scans is was also determined that the level surface length within the adhesive print between the lateral edges 116 increased 2 to 4 mils. Although the angles and definition increases from these scans are specifically for Ablestick® XR-

41395-10 with a viscosity of 40,000 cps, thixotropic index of 3.6, and a baking profile of 30 minutes at 125°C, 30 minutes at 200°C, and 30 minutes ramping from 200°C to 245°C, comparable results have been achieved for OxyChem® 2421-A6-sp 7495-128B with a viscosity of 46,000 cps, thixotropic index of 1.35, and a baking profile of 60 minutes at 120°C and 180 minutes at 190°C. Thus, the graphs shown in FIGs. 6-14 illustrate the general improvement trend which will be achieved through the use of the present invention.

As shown in FIGs. 15-17, adhesive coated leadfingers for LOC attachment can be formed by the inversion method of the present invention. An adhesive material 202 is applied, generally by spray application, on an attachment surface 204 of a leadfinger 206, as shown in FIG. 15. After application of the adhesive material 202, the leadfinger 206 is inverted, as shown in FIG. 16. By inverting the leadfinger 206, the adhesive material 202 will not flow down the sides 208 of the leadfinger 206 and, of course, will not collect on the bond wire surface 210 of the leadfinger 206, as shown in FIG. 17. Since the adhesive material 202 does not collect on the bond wire surface 210, there will be no adhesive material 202 to interfere with the subsequent wirebonding step subsequent to LOC attachment of the active surface of the die to the leads.

FIG. 18 illustrates an encapsulated semiconductor device 302 made by the inversion method of the present invention. As discussed above and illustrated in FIGs. 34-36, a stencil 802 is placed on a conductive-carrying substrate, such as a PCB 804, such that a cavity 806 in the stencil 802 exposes a semiconductor device 808 to be encapsulated and a portion of the substrate or PCB 804 surrounding the semiconductor device 808, as shown in FIG. 34. An encapsulant material 810, such as silicone, polyimide, urethane, acrylic, epoxy, plastic, and the like, is then extruded from a nozzle 812 into the stencil open area 806, as shown in FIG. 35. When the stencil 802 is removed, the substrate or PCB 804 is inverted to prevent the encapsulant material 810 from spreading or flowing laterally under the force of gravity. By preventing the flow of the encapsulant material 810, the encapsulant

material 810 on the top surface 814 of the semiconductor device 808 remains thick enough to provide adequate protection for the semiconductor device 808.

FIGs. 19-21 illustrate the formation of traces on a semiconductor substrate by the method of the present invention. A stencil or print screen 402 with an appropriate trace design is placed over a semiconductor substrate 404, as shown in FIG. 19. A conductive material 406 is applied to the stencil or print screen 402, as shown in FIG. 20. The stencil or print screen 402 is then removed leaving conductive traces 408, and the semiconductor substrate 404 is inverted during the drying or curing of the conductive traces 408, as shown in FIG. 21. Since the conductive material 406 is prevented from flowing laterally by the inversion of the semiconductor substrate 404, the distance between parallel conductive traces 408 can be reduced resulting in a reduction of the size of the semiconductor substrate.

FIG. 22 illustrates conductive polymer bumps 502 formed by the method of the present invention. As previously discussed and illustrated in FIGs. 41-43, the conductive polymer bumps 1002 are generally formed on bond pads 1004 on the surface of a semiconductor substrate 1006. The bond pads 1004 are in electrical communication with integrated circuitry (not shown) on or in the semiconductor substrate 1006 via electrical traces 1008 in or on the semiconductor substrate 1006. As shown in FIG. 41, a print screen or stencil 1010 is placed over the semiconductor substrate 1006 with openings 1012 over each bond pad 1004. The conductive polymer is deposited in the openings 1012, as shown in FIG. 42. The print screen or stencil 1010 is removed and the semiconductor substrate 1006 inverted to maintain the definition of the conductive polymer bumps 502, as shown in FIG. 22. With the present invention, the conductive polymer bumps 502 can achieve height to width ratios of the preferred target of 3:1 or greater, since the weight of the polymer material causing the conductive polymer bump 502 to collapse on itself and flow or spread is no longer an issue. It is also understood that the inversion method of the present invention could also be used in the formation of metallic conductive bumps.

* * * * *

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A method of controlling the spread of a material deposited on a semiconductor device component, comprising:

providing said semiconductor device component;

depositing said material on said semiconductor device component; and

inverting said semiconductor device component until said material obtains a desired stable shape and boundary definition of said deposited material.

2. A method of controlling definition of surface features of a material deposited on a semiconductor device component, comprising:

providing said semiconductor device component;

depositing said material on said semiconductor device component; and

inverting said semiconductor device component until said material obtains a desired stable shape and boundary definition of said deposited material.

3. A method of controlling the angle of repose of a material deposited on a semiconductor device component, comprising:

providing said semiconductor device component;

depositing said material on said semiconductor device component; and

inverting said semiconductor device component until said material obtains a desired stable angle of repose of said deposited material.

4. A method of forming an adhesive patch, comprising:

providing a semiconductor substrate;

depositing an adhesive material on said semiconductor substrate; and

inverting said semiconductor substrate until said adhesive material obtains a desired stable shape and boundary definition of said deposited adhesive material.

5. The method of claim 4, wherein depositing said adhesive material, includes:

placing a template, having at least one aperture, on said semiconductor substrate;

depositing said adhesive material into said template aperture; and

removing said template.

6. The method of claim 4, wherein said semiconductor substrate includes a flip-chip used in an lead-on-chip attachment configuration.

7. A semiconductor substrate having at least one adhesive patch formed by:

providing a semiconductor substrate;

depositing an adhesive material on said semiconductor substrate; and

inverting said semiconductor substrate until said adhesive material obtains a desired stable shape and boundary definition of said deposited adhesive material.

8. The semiconductor substrate of claim 7, wherein depositing said adhesive material, includes:

placing a template, having at least one aperture, on said semiconductor substrate;

depositing said adhesive material into said template aperture; and

removing said template.

9. A method of forming a conductive bump, comprising:

providing a semiconductor substrate having at least one bond pad;

forming a conductive bump on said semiconductor substrate bond pad with a conductive material; and

inverting said semiconductor substrate until said conductive material obtains a desired stable shape and boundary definition of said deposited conductive material.

10. The method of claim 9, wherein forming said conductive bump includes:

placing a template, having at least one aperture, on said semiconductor substrate;

depositing said conductive material into said template aperture; and

removing said template.

11. The method of claim 9, wherein said semiconductor substrate includes a printed circuit board.

12. The method of claim 9, wherein said semiconductor substrate includes a flip-chip.

13. A printed circuit board having at least one conductive bump formed by:

providing said printed circuit board with at least one bond pad;

forming a conductive bump on said printed circuit board bond pad with a conductive material; and

inverting said printed circuit board until said conductive material obtains a desired stable shape and boundary definition of said deposited conductive material.

14. The method of claim 13, wherein forming said printed circuit board includes:

placing a template, having at least one aperture, on said printed circuit board;

depositing a conductive material into said template aperture; and

removing said template.

15. A flip-chip having at least one conductive bump formed by:
providing said flip-chip with at least one bond pad;
forming a conductive bump on said flip-chip bond pad with a conductive material; and
inverting said flip-chip until said conductive material obtains a desired stable shape and boundary definition of said deposited conductive material.

16. The method of claim 15, wherein forming said conductive bump includes:
placing a template, having at least one aperture, on said flip-chip;
depositing a conductive material into said template aperture; and
removing said template.

17. A method of forming an encapsulant on a semiconductor device, comprising:
providing a semiconductor substrate having a semiconductor device attached thereto;
depositing an encapsulant material on said semiconductor device and on a portion of said semiconductor substrate; and
inverting said semiconductor substrate until said encapsulant material obtains a desired stable shape and boundary definition of said deposited encapsulant material.

18. The method of claim 17, wherein said portion of said semiconductor substrate includes an area about a periphery of said semiconductor device.

19. The method of claim 17, wherein depositing said encapsulant material includes:

placing a template, having at least one aperture, on said semiconductor substrate wherein said aperture exposes said semiconductor device and said portion of said semiconductor substrate;

depositing said encapsulant material into said template aperture; and

removing said template.

20. A method of forming an adhesive coated lead frame, comprising:

providing a lead frame having at least one lead finger;

depositing an adhesive material on a portion of an attachment surface of said lead finger; and

inverting said lead frame until said adhesive material obtains a desired stable shape and boundary definition of said deposited adhesive material.

21. An adhesive coated lead frame formed by:

providing a lead frame having at least one lead finger;

depositing an adhesive material on a portion of an attachment surface of said lead finger; and

inverting said lead frame until said adhesive material obtains a desired stable shape and boundary definition of said deposited adhesive material.

22. A method of forming a conductive trace, comprising:

providing a semiconductor substrate;

forming a conductive trace on said semiconductor substrate with a conductive material; and

inverting said semiconductor substrate until said conductive trace obtains a desired stable shape and boundary definition of said deposited conductive trace.

23. The method of claim 22, wherein forming said conductive trace includes:

placing a template, having at least one aperture with a desired shape of said conductive trace, on said semiconductor substrate;

depositing said conductive material into said template aperture; and

removing said template.

24. The method of claim 22, wherein said semiconductor substrate includes a printed circuit board.

ABSTRACT

A method of forming high definition elements for electrical and electronic devices, substrates, and other components from or including viscous material. The method includes inverting the electrical components after the viscous material is applied and maintaining the inverted orientation until the viscous material dries or cures enough to maintain definition of its perimeter and edge characteristics.

N:\C\2269\2911.PAT

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Tongbi Jiang; Syed S. Ahmad

Serial No.: To be assigned

Filed: April 21, 1999

For: GRAVITATIONALLY-ASSISTED CONTROL OF SPREAD OF VISCOUS MATERIAL APPLIED TO SEMICONDUCTOR ASSEMBLY COMPONENTS

Examiner: To be assigned

Group Art Unit: To be assigned

Attorney Docket No.: 2911.1US
(96-436.1)

NOTICE OF EXPRESS MAILING
Express Mail Mailing Label Number: EL248175219US
Date of Deposit with USPS: April 21, 1999
Person making Deposit: Jared Turner

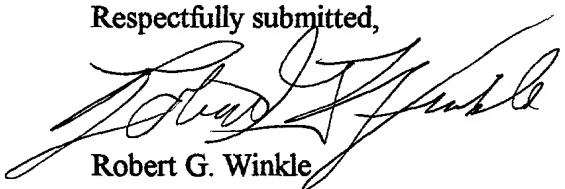
TRANSMITTAL OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Attn: Official Draftsperson
Drawing Review Branch
Washington, D.C. 20231

Sir:

Enclosed for filing are (17) sheets with 43 total FIGs. of formal drawings which are being submitted within the time period set by the allowance notice.

Respectfully submitted,



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Registration No. 37,474
Attorney for Applicants
TRASK, BRITT & ROSSA
P. O. Box 2550
Salt Lake City, UT 84110

Date: April 21, 1999
Enclosed: 17 sheets of formal drawings
RGW/kf

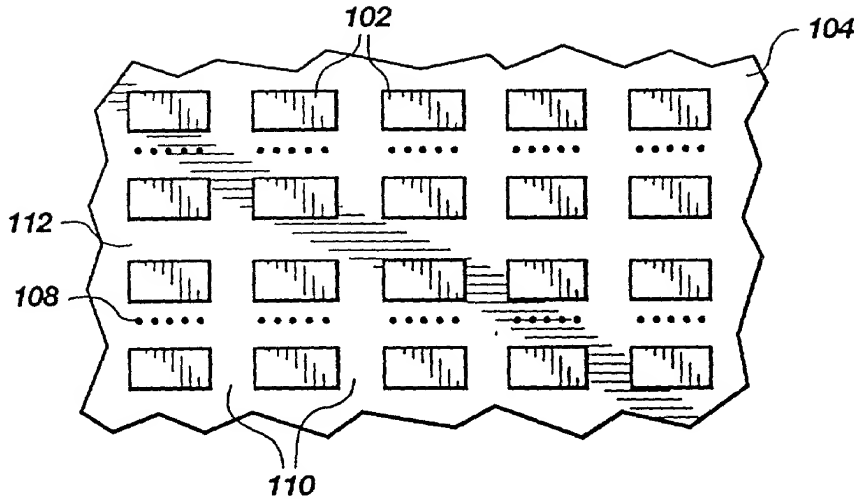


Fig. 1

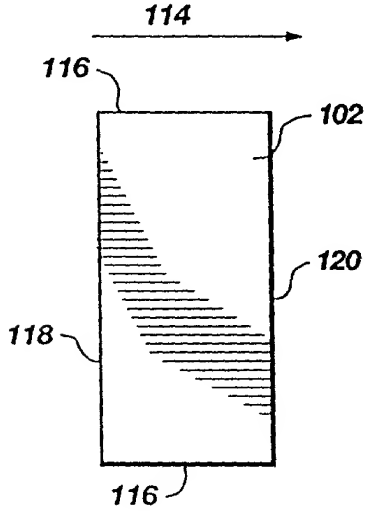


Fig. 2

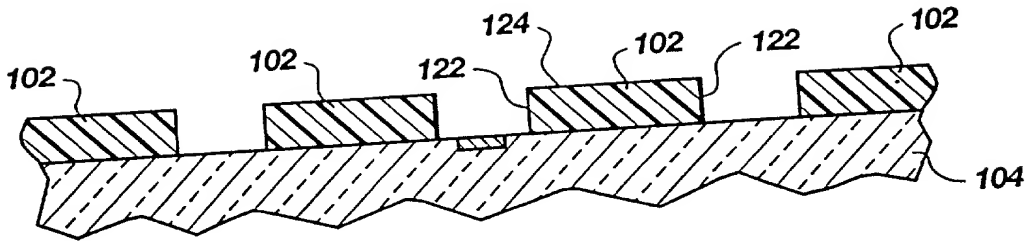


Fig. 3

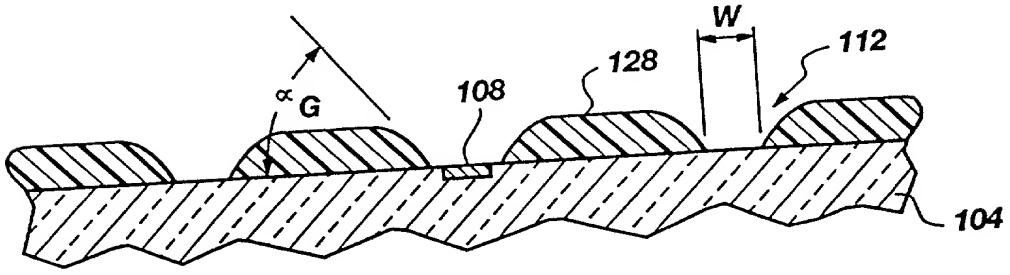


Fig. 4

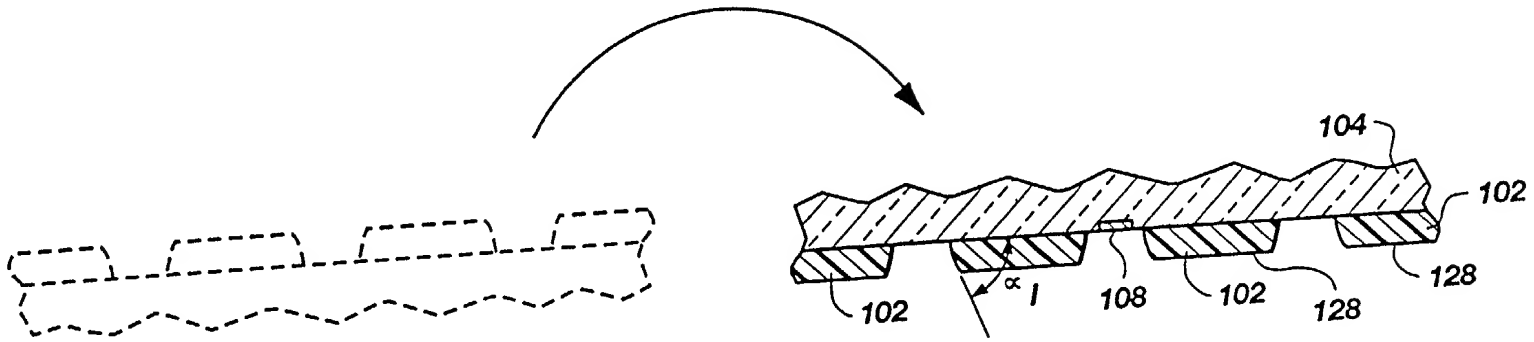


Fig. 5

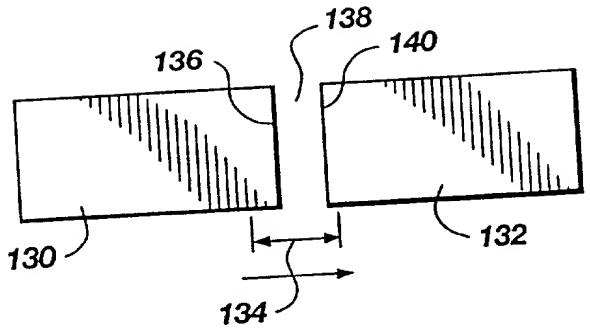


Fig. 6

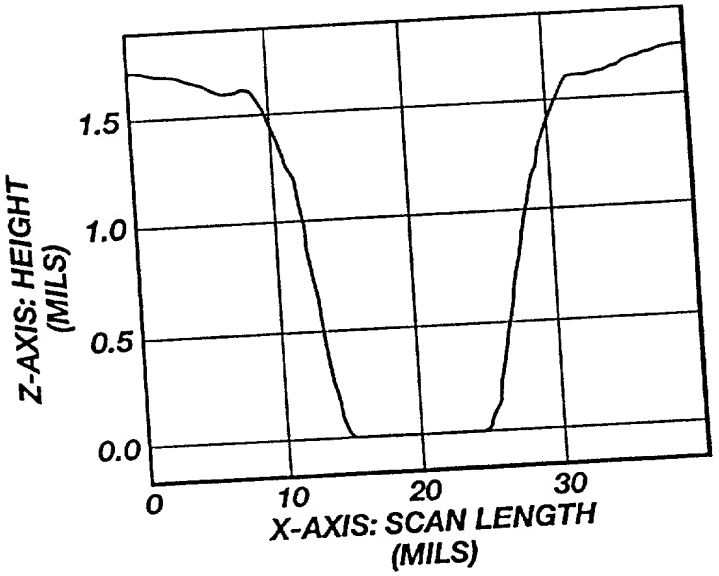


Fig. 7

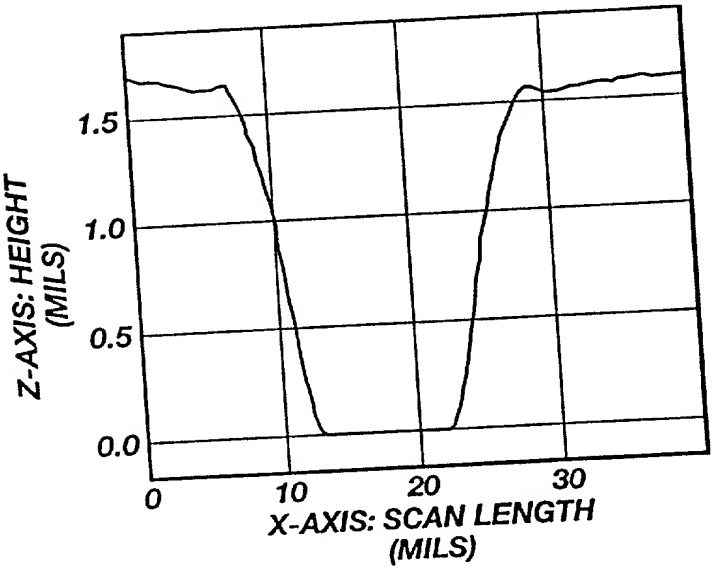


Fig. 8

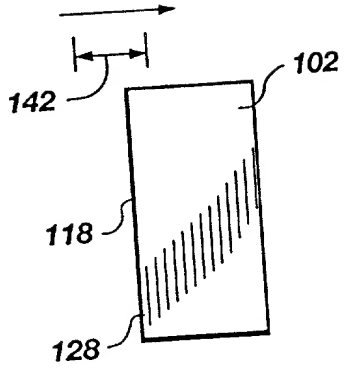


Fig. 9

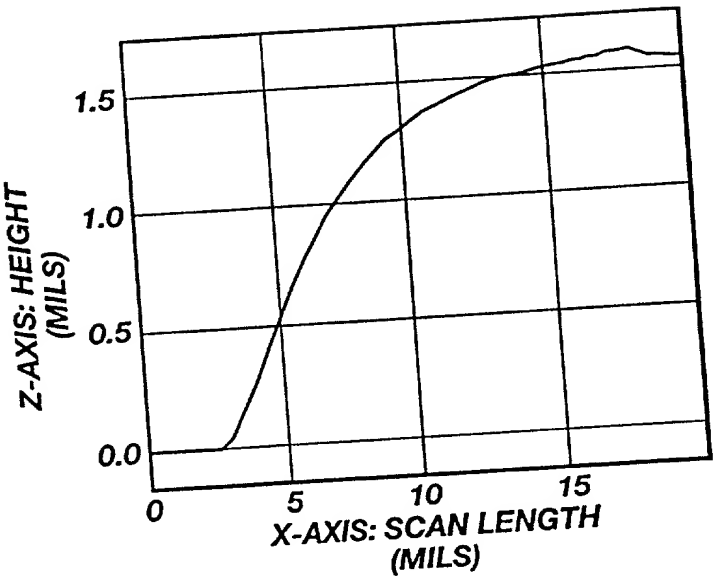


Fig. 10

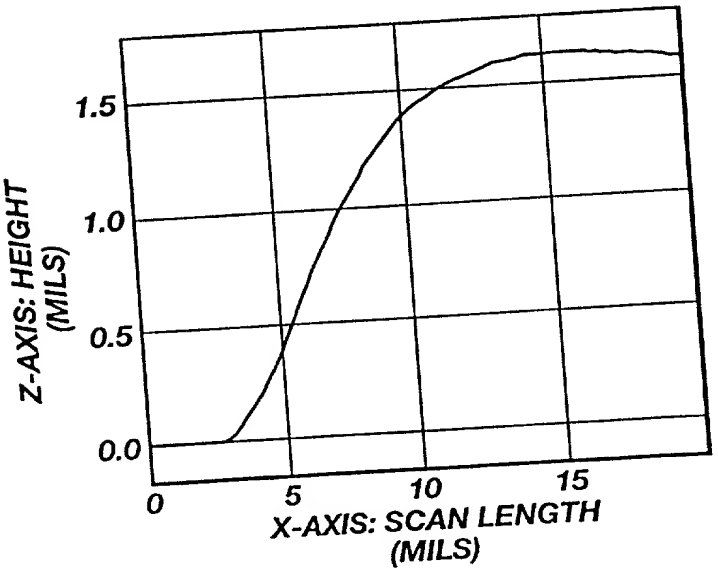


Fig. 11

Fig. 12

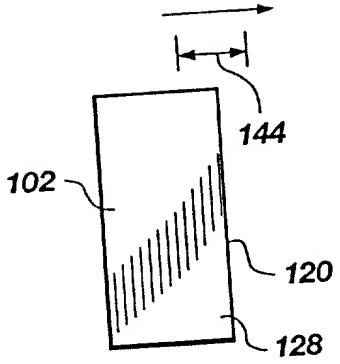


Fig. 13

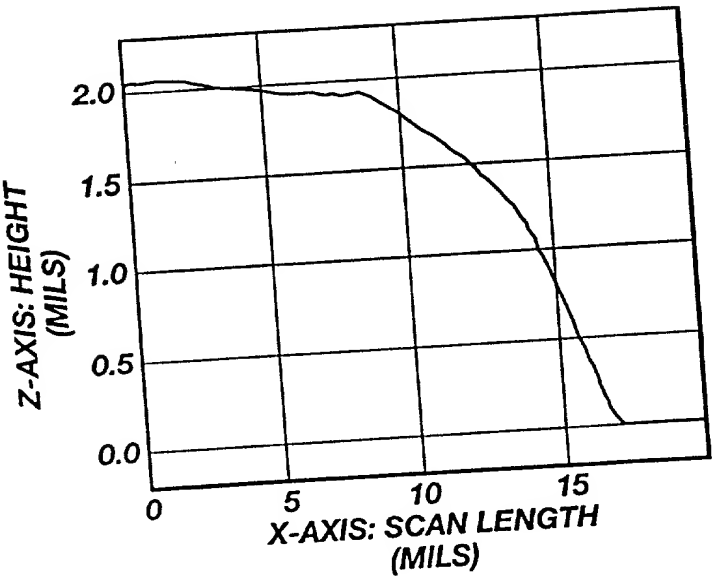
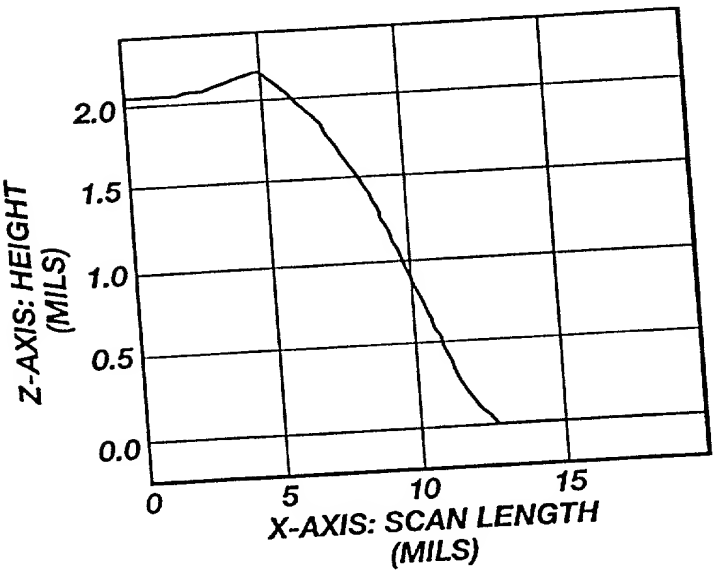


Fig. 14



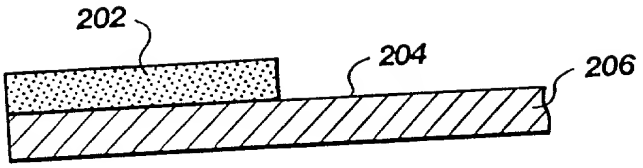


Fig. 15

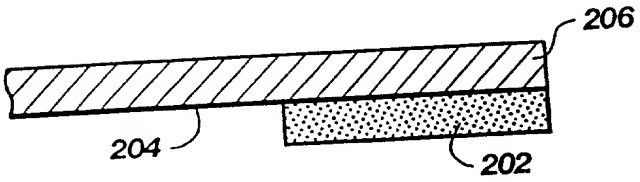


Fig. 16

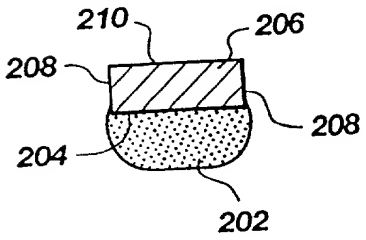


Fig. 17

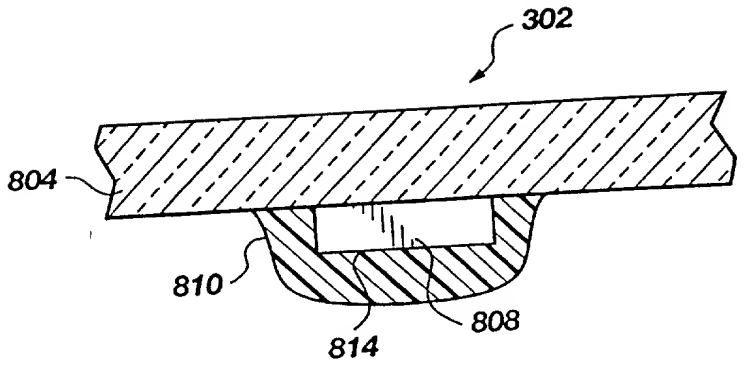


Fig. 18

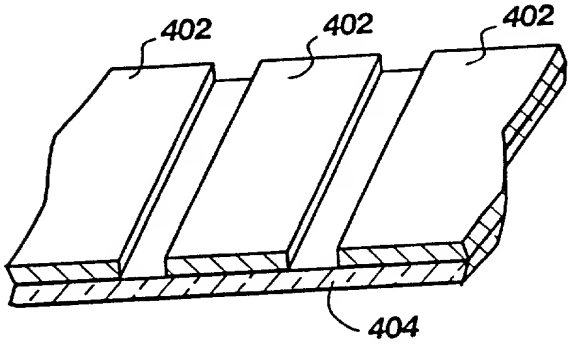


Fig. 19

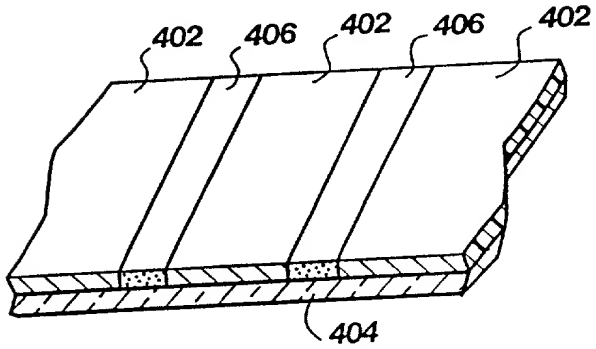


Fig. 20

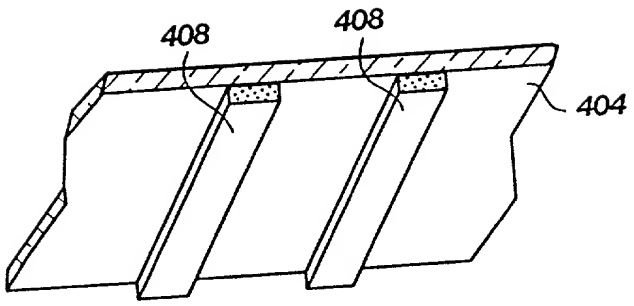


Fig. 21

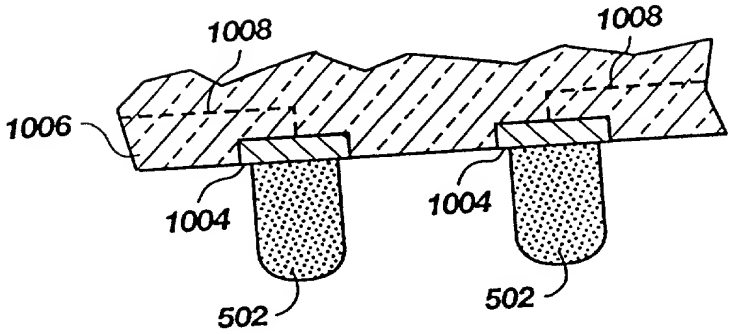


Fig. 22

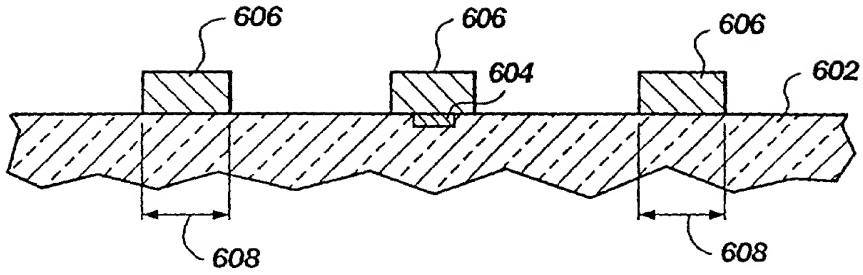


Fig. 23

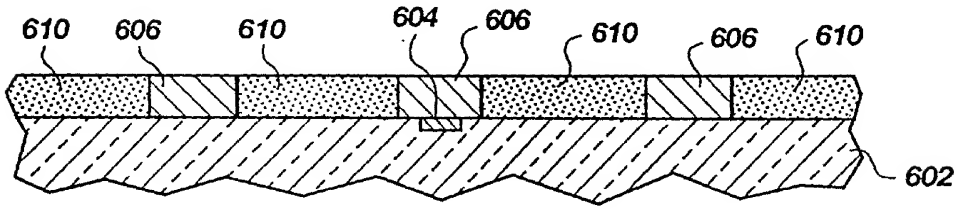


Fig. 24

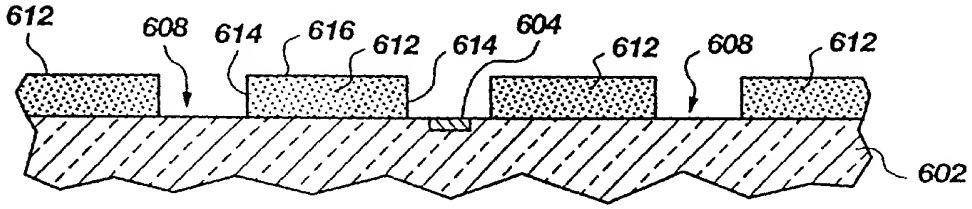


Fig. 25

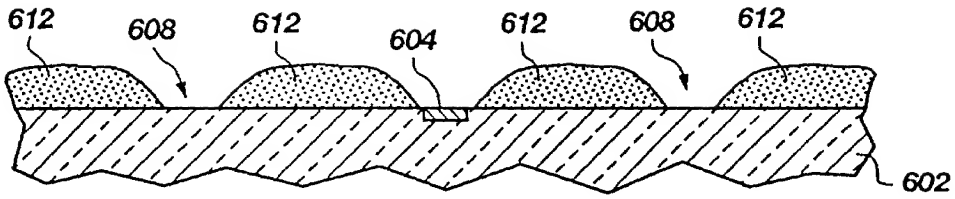


Fig. 26

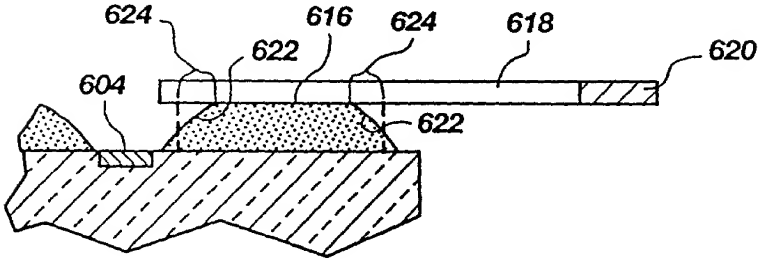


Fig. 27

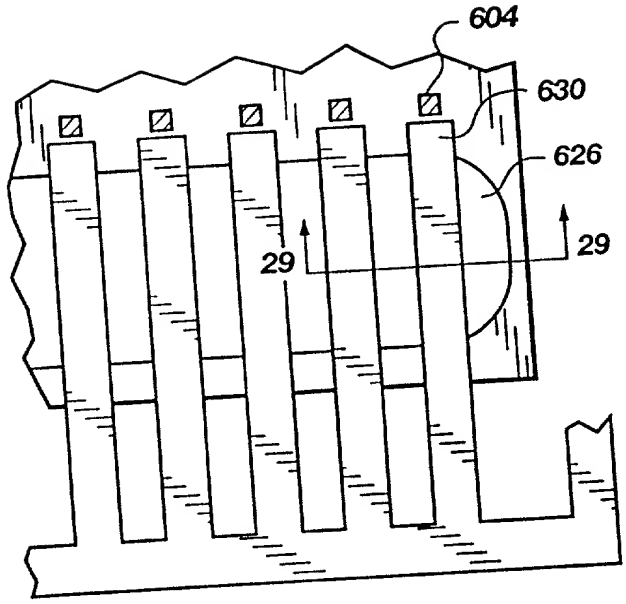


Fig. 28

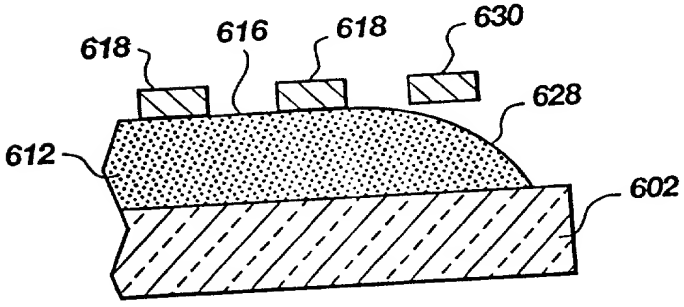


Fig. 29

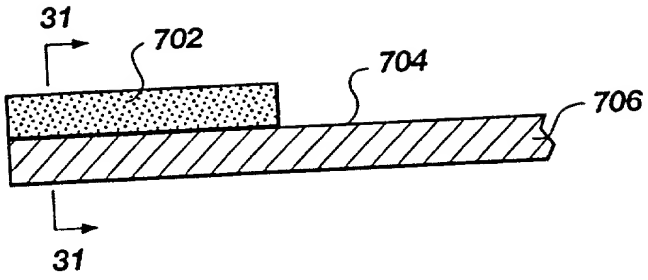


Fig. 30

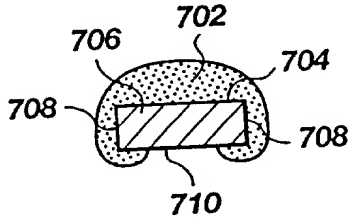


Fig. 31

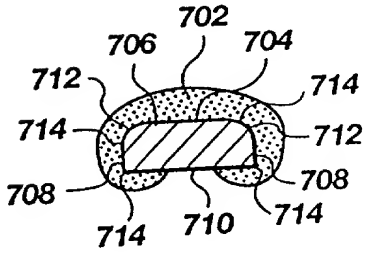


Fig. 32

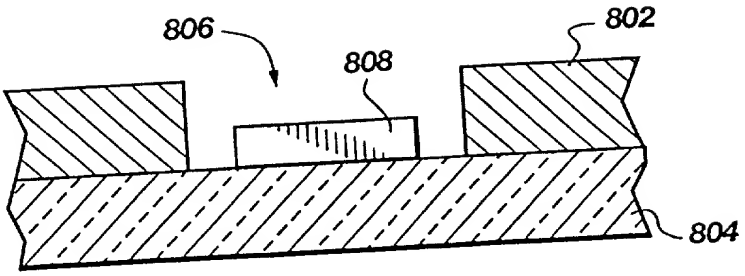


Fig. 33

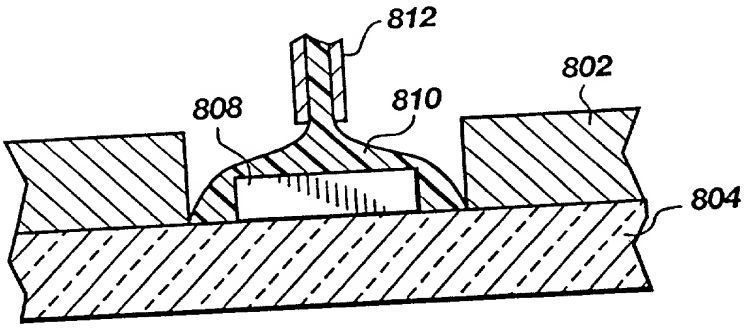


Fig. 34

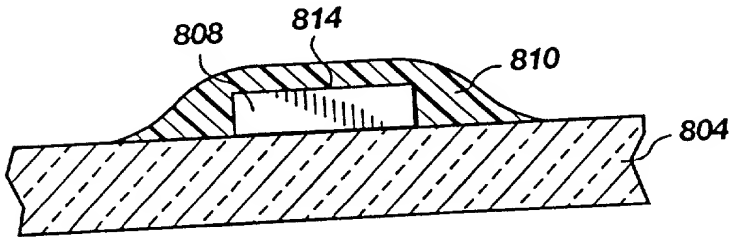


Fig. 35

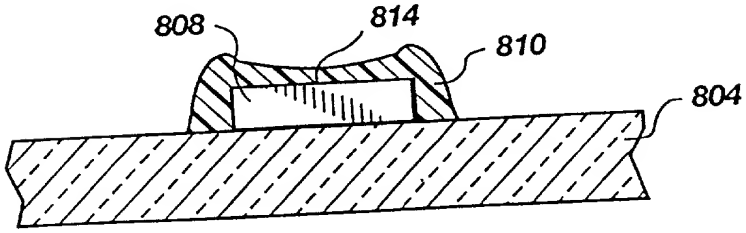


Fig. 36

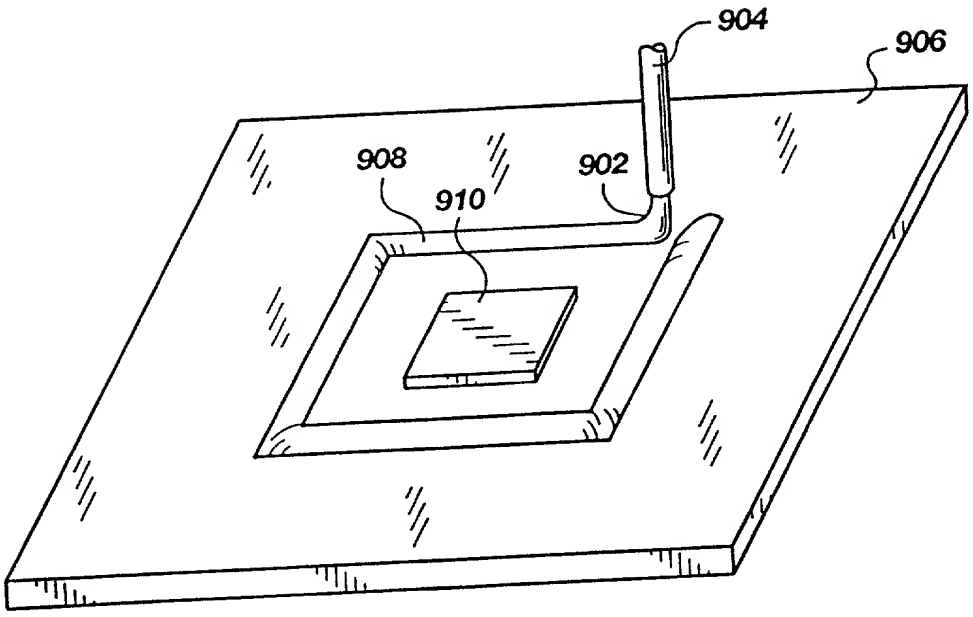


Fig. 37

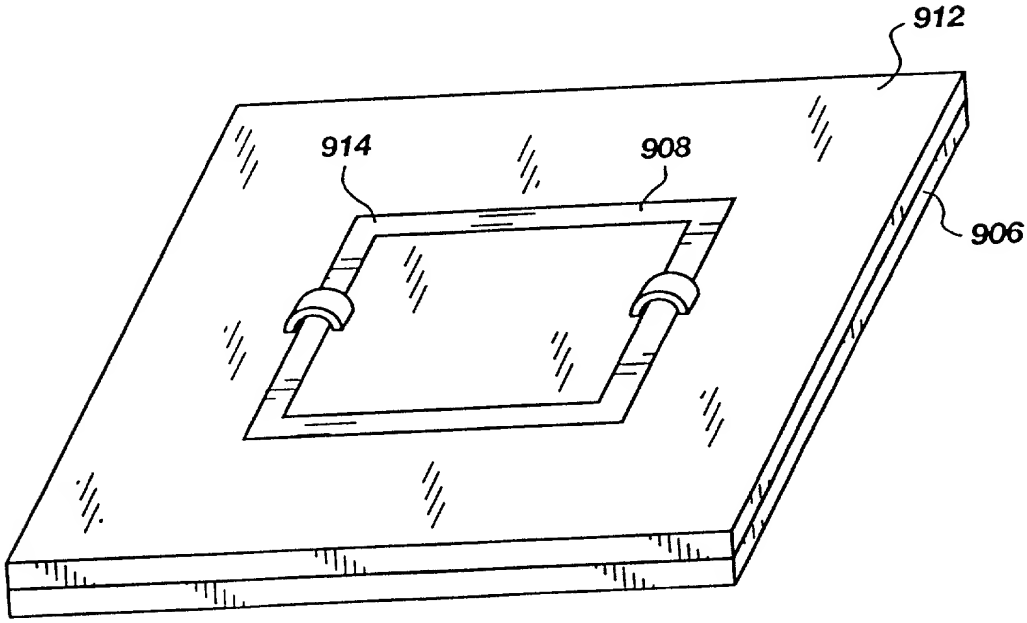


Fig. 38

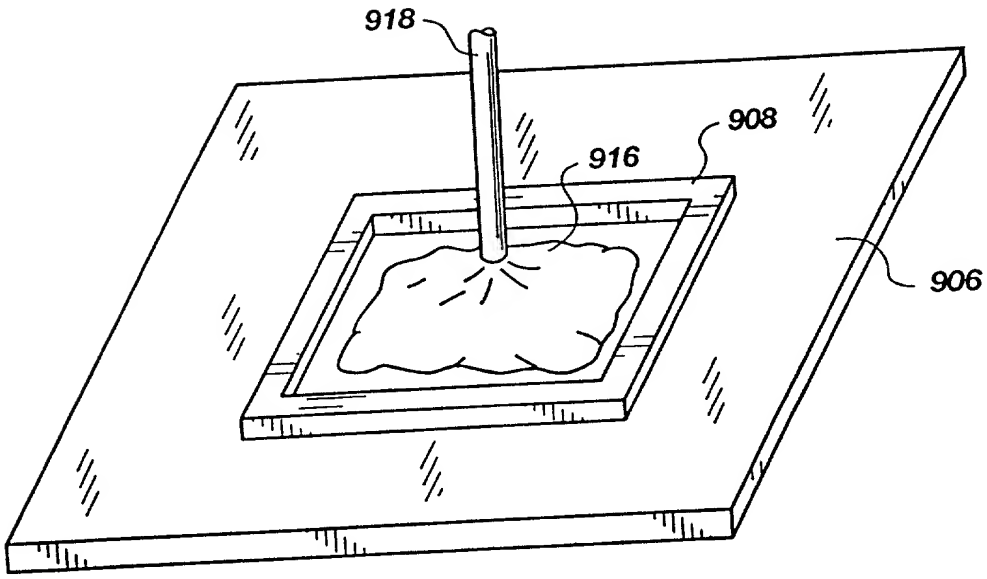


Fig. 39

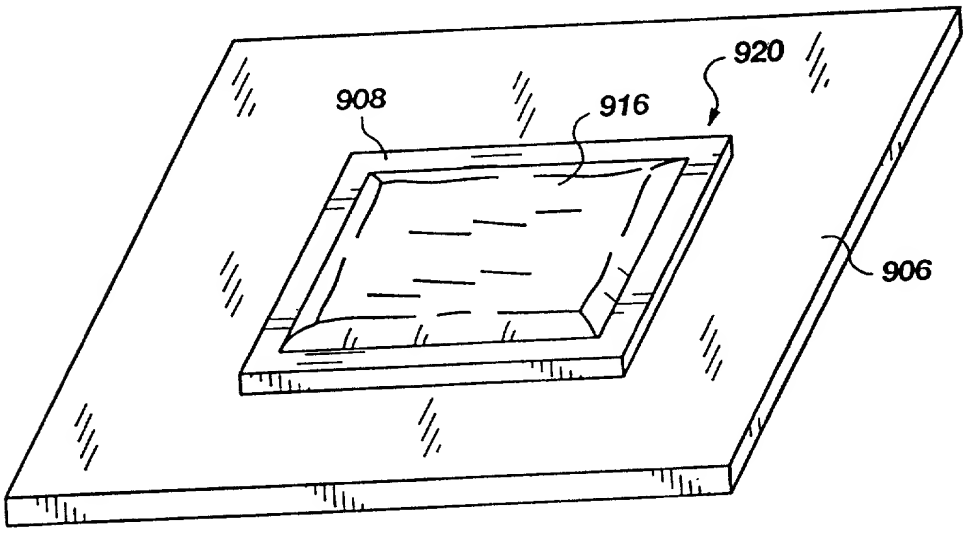


Fig. 40

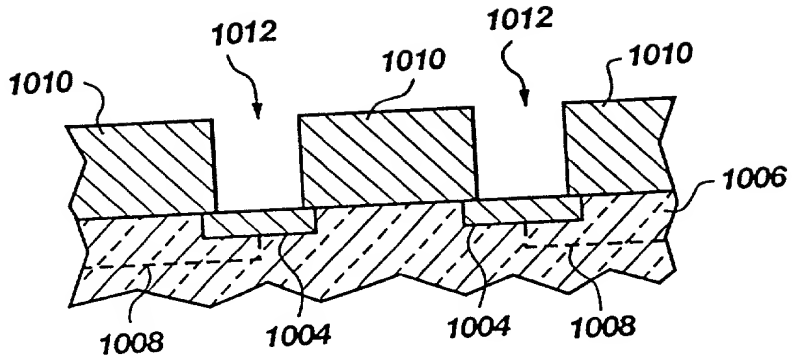


Fig. 41

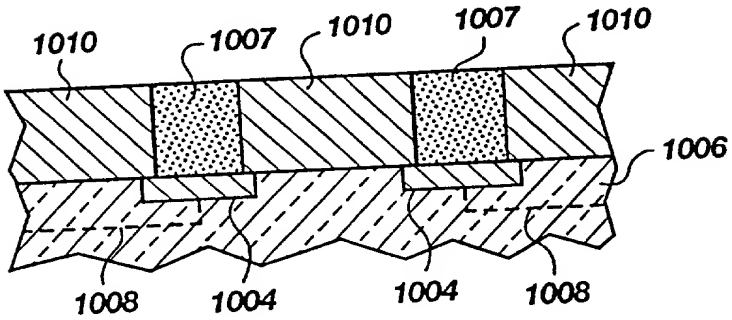


Fig. 42

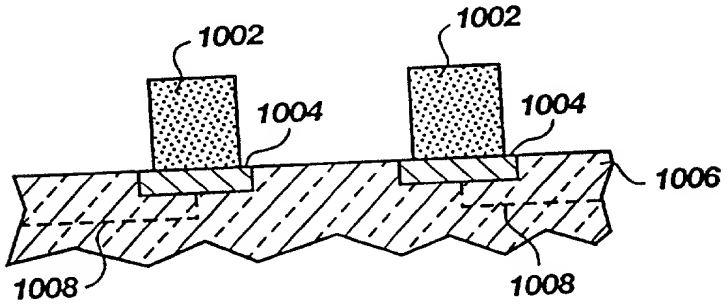


Fig. 43

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled GRAVITATIONALLY-ASSISTED CONTROL OF SPREAD OF VISCOUS MATERIAL APPLIED TO SEMICONDUCTOR ASSEMBLY COMPONENTS, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability is defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
(provisional application no.)	(filing date)
(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: Tongbi Jiang
Inventor's signature _____ Date Sept 9/4/96
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DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention title: GRAVITATIONALLY-ASSISTED CONTROL OF SPREAD OF VISCOUS MATERIAL APPLIED TO SEMICONDUCTOR ASSEMBLY COMPONENTS

Inventor name(s) appearing on first declaration page: Tongbi Jiang

☒ Additional original, first and joint inventor(s):

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Inventor's signature Syed Sajid Ahmad Date 8/4/96
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